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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 828
BLOOMFIELD HILLS, MI 48303

EXAMINER	
VILLECCO, JOHN M	
ART UNIT	**PAPER NUMBER**
2622	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/763,121	NASU, HIROAKI	
	Examiner	Art Unit	
	John M. Villecco	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The prosecution of this application has been transferred to Examiner John M. Villecco from the docket of Examiner Scott Egan. Any inquiry concerning this Office Action or earlier communications should be directed to the current Examiner of record. Current contact information is provided in the last section of this communication.

Response to Arguments

2. Applicant's arguments filed July 25, 2007 have been fully considered but they are not persuasive.

3. Regarding claim 1, applicant argues that Tsang fails to disclose that the circuit for changing a gate applied voltage applies at least one of a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in an accumulation state and another predetermined voltage from a second voltage source to the gates of the plurality of transistors while in a reading out state. In support of this assertion, applicant contends that Tsang fails to disclose the limitation of applying another predetermined voltage from a second voltage source to the gates of the transistors while in a reading out state. Applicant states that the transistors of Tsang are always connected to the same source. See the arguments presented on page 7 of the response.

4. The examiner maintains that based upon the broad wording recited in claim 1, Tsang can be read on the claimed invention. More specifically, attention is directed toward the wording "at least one of" in line 11 of the amended claims. This claim phrasing makes it clear that only one

of a first predetermined voltage from a first voltage source ***OR*** a second predetermined voltage from a second voltage source needs to be applied to the gates of the transistors. Therefore, since it is clear that a first predetermined voltage (for instance, SC) is being applied to the gate of the transistors (for instance, N2), then the Tsang reference meets the claimed limitation. In other words, since the applicant has used the claim language "at least one of", only one of the first and second voltages from first and second sources has to be met.

5. Furthermore, even if the second limitation of the "at least one of" terminology had to be met. The examiner contends that Tsang can still be read on the broadly claimed wording. More specifically, applicant claims "a circuit for changing a gate-applied voltage that changes a voltage applied ***to each gate of a plurality of the transistors***", "wherein the circuit for changing a gate-applied voltage applies at least one of a predetermined voltage ***to each gate of a plurality of the transistors***...and another predetermined voltage from a second voltage source ***to the gates of the plurality of transistors***" (emphasis added). This wording indicates that a circuit changes the voltage applied to each of a plurality of transistors. This does not mean that the voltage applied, is applied to all of the transistors. It only has to be applied to the gates of the plurality of transistors. Therefore, since Tsang teaches that a voltage applied to a plurality of transistors can be regulated (for instance, Fig. 7 shows that the voltage SC is modulated over time, wherein the plurality of transistors is each of the N2 transistors in each pixel). Furthermore, Tsang discloses two different voltage sources (SC and RS, for example) applied to the plurality of transistors. Secondly, Tsang teaches a second voltage (RS) applied to the gates of the plurality of transistors (N5 in each of the pixels). Thus, the plurality of transistors do not have to be same transistors, as interpreted by the examiner. They merely have to be contained in the same group of transistors.

In this case, the group of transistors are all of the transistors includes in all of the pixels. Therefore, a first voltage is applied to each gate of a plurality of the transistors and a second voltage is applied to the gates of the plurality of transistors.

6. The rejection of claim 5 can be maintained similarly to the argument provided above.

7. As for claim 6, applicant has amended the claim to include the limitation of "wherein the circuit for changing gate-applied voltage selectively applies the first and second voltage outputs based on an accumulation enable signal and a reading out enable signal, respectively. It is noted that the claim 6 also includes the claim terminology of applying "at least one of" the first and second voltages. Thus, only one or the other has to be met in the prior art. Furthermore, since the newly added limitation depends on whether the first or second voltage is applied, only the accumulation enable signal or the reading out enable signal has to be met. Furthermore, the examiner contends that Tsang discloses that the voltage applied depends on an accumulation enable signal (ISC). Please see the newly worded grounds of rejection on the following pages.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsang et al. (U.S. Patent No. 5,900,623).

10. Regarding ***claim 1***, Tsang teaches an image-processing device (fig 4) comprising: a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4); a circuit for changing a gate-applied voltage that changes a voltage applied to each gate of a plurality of the transistors (fig 4, each gate is connected to a voltage signal that is changed according to the timing diagram in fig 7); wherein the circuit for changing a gate-applied voltage applies at least one of a predetermined voltage to each gate of a plurality of the transistors from the first voltage source while in an accumulation state (the timing diagram in fig 7 shows the voltages on each transistor during integration, see ROW and SC voltages) when carriers are generated from the photo diode in response to received light, and another predetermined voltage from the second voltage source while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the voltages on each transistor during readout, see ROW and SC voltages), (see also column 7, lines 28-57). Furthermore, attention is directed toward the wording "at least one of" in line 11 of the amended claims. This claim phrasing makes it clear that only one of a first predetermined voltage from a first voltage source ***OR*** a second predetermined voltage from a second voltage source needs to be applied to the gates of the transistors. Therefore, since it is clear that a first predetermined voltage (for instance, SC) is being applied to the gate of the transistors (for instance, N2), then the Tsang reference meets the claimed limitation. In other words, since the applicant has used the claim language "at least one of", only one of the first and second voltages from first and second sources has to be met.

11. As for ***claim 2***, Tsang discloses wherein the circuit for changing a gate-applied voltage applies a third predetermined voltage to each gate of a plurality of the transistors from the third voltage source while in a clearing state when residual carriers in the solid-state image pickup device are excluded from the solid-state image pickup device (the timing diagram in fig 7 show the voltages on each transistor during reset, see ROW, SC, and RS), (see also column 10, lines 12-18).

12. With regard to ***claim 3***, Tsang discloses a plurality of gate voltage supplying circuits coupled to the gates of a plurality of the transistors (SC, RS, and ROW, fig 4); wherein the changed applied voltage is applied to a plurality of the gate voltage supplying circuits from the circuit for changing a gate-applied voltage (the timing diagram in fig 7 shows the change in voltages on the transistors during different phases).

13. Regarding ***claim 4***, Tsang discloses a plurality of gate voltage supplying circuits coupled to the gates of a plurality of the transistors (SC, RS, and ROW, fig 4); wherein each of a plurality of the gate voltage supplying circuits includes the circuit for changing a gate-applied voltage (the timing diagram in fig 7 shows the change in voltages on the transistors during different phases).

14. As for ***claim 5***, Tsang discloses a method of image-processing that picks up an image with a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4), the method comprising: applying a predetermined voltage to each gate of a plurality of the transistors from a first voltage source while in an accumulation state when carriers are generated from the photo diode in response to received light

(the timing diagram in fig 7 shows the change in voltages on each transistor during integration, see ROW and SC voltages); and applying a predetermined voltage to each gate of a plurality of the transistors from a second voltage source while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the change in voltages on each transistor during readout, see ROW and SC voltages).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsang et al. (U.S. Patent No. 5,900,623).

17. Regarding ***claim 6***, Tsang teaches an image-processing device (fig 4) comprising: a solid-state image pickup element (active pixel sensor, column 4, lines 1-3) provided with a plurality of unit pixels (fig 4 demonstrates a pixel in the active pixel array), each unit pixel including a photo diode (photodiode PD, fig 4) and a plurality of transistors for detecting an optical signal (MOS transistors N1-N5, fig 4); a circuit for changing a gate-applied voltage that changes a voltage applied to each gate of a plurality of the transistors (fig 4, each gate is connected to a voltage signal that is changed according to the timing diagram in fig 7); wherein the circuit for changing a gate-applied voltage applies at least one of a predetermined voltage to each gate of a plurality of the transistors from the first voltage source while in an accumulation state (the timing diagram

in fig 7 shows the voltages on each transistor during integration, see ROW and SC voltages) when carriers are generated from the photo diode in response to received light, and another predetermined voltage from the second voltage source while in a reading out state when a signal in response to carriers accumulated in the accumulation state is read out (the timing diagram in fig 7 shows the voltages on each transistor during readout, see ROW and SC voltages), (see also column 7, lines 28-57). Additionally, Tsang discloses the use of an ISC signal (integration mode signal) during accumulation period to being integration. This is interpreted to be the accumulation enable signal. Furthermore, attention is directed toward the wording "at least one of" in line 11 of the amended claims. This claim phrasing makes it clear that only one of a first predetermined voltage from a first voltage source ***OR*** a second predetermined voltage from a second voltage source needs to be applied to the gates of the transistors. Therefore, since it is clear that a first predetermined voltage (for instance, SC) is being applied to the gate of the transistors (for instance, N2), then the Tsang reference meets the claimed limitation. In other words, since the applicant has used the claim language "at least one of", only one of the first and second voltages from first and second sources has to be met.

However, Tsang et al. does not explicitly teach the use of a regulator that produces several voltages, which are then used on the transistors. Official Notice is taken that both the concept and the advantages of providing a regulator to provide different voltage values to different destinations from one source is well known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a regulator in the active pixel sensor found in Tsang et al. as regulators are known to stabilize a desired voltages on multiple paths.

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John M. Villecco whose telephone number is (571) 272-7319. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John M. Villecco
Primary Examiner, Art Unit 2622
October 11, 2007